**NUS ISS Master of Technology**

**CAPSTPONE PROJECT PROPOSAL**

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| **Date of proposal:**  22 Nov 2019 |
| **Project Title:**  Chamber Test Fallout Classifier and Analyzer |
| **Sponsor/Client:** *(Company, Name, Address, Telephone No. and Contact Name)*  *For student conceived project, put the name(s) of the team members*  *Micron Technology*  *Ong Boon Ping*  *990, Bendemeer Road, Singapore 330942*  *Handphone No: 90619483* |
| **Background/Aims/Objectives:**  *Provide a brief* ***background*** *of the project including a description of the domain and* ***problem*** *area.*  *In electronic industry, IC testing can be performed before or after assembly.*  *After fabrication, wafer will be tested. Wafer testing will be ran before wafer cutting and after the IC assembly steps.*  *After each IC is assembled, backend testing of the IC begins.*  *This project is aimed to create a system that recognize failing pattern in chamber testing after assembly process.*  *The recognized failing patterns enable further root cause analysis.*  *Classification of potential root cause can be done based on statistics or record at each manufacturing or purchasing records. The identified causes can be used to trigger the process refinement.*  *The problem is to identify genuine chamber test fails and give alarm on false chamber test fallouts. Actions can be trigger to either vendor or engineering departments.*  *Major challenge is to automate the process using pattern recognition system with acceptable accuracy in noisy manufacturing or testing environment.*  ***Objective(S)***  *Subsequently, describe the aim and objective of the specific project for the students.*  The aim is to give overall report on anomalies found in chamber testing, give alarm to the respective engineers to refine chamber testing or material enhancement.  The objectives are:   1. Identify genuine chamber fails that corresponds to certain spatial wafer region. The expected outcome is trigger fabrication process enhancement.   Edge, center, doughnut and other fail cluster at the wafer usually corresponds fabrication fails. The identification of fail region enable further correlation of failing region to problematic processes.    The identification of wafer failing pattern at chamber testing step. Edge, center and other defects that can be detected on the wafer. (Each colored bit represented 1 IC chip based on its location on wafer before it is cut, assembled and packaged)   |  |  | | --- | --- | | **Wafer Fail Region** | **Common Process Defects** | | Center | Wafer crystal defect (Resistance data of different wafer)  Vendor Issue (Vendor record of each wafer) | | Edge | Cutting (Cutting machine records)  Grinding (Grinding machine records) | | Cluster | Contamination (Clean room record)  Photolithography(X-ray records) | | Doughnut | Hot Ion Injection (Machine record)  Chemical Vapor Disposition Issue (Machine record) |   Common defects of each wafer fail region. After identifying the wafer region with chamber fails concentrated, statistical data of each process at the concentrated region can be analyzed and narrow down to the exact defects.   1. Identify false chamber fails that generated by chamber testing equipment. This is to identify the faulty equipment and trigger repair.   The IC will be loaded on PCB testing board before testing. Testing location on PCB testing board will affect the testing results due to uneven temperature/moisture. Hence, such non-conformance must be controlled.  Chamber tests that are related to the temperature corner can be identified by analyzing time series data coming from temperature sensors.    Identification of chamber test failing pattern on PCB test board by neural network (variational autodecoder)  Hotter color indicates higher fuzzy probabilities in having PCB test board related issue. The convolutional filter size can be set based on electrical routing on the PCB test board.  Feedback can be sent to PCB test board manufacturer to enhance the PCB signal integrity.   |  |  | | --- | --- | | **PCB Defect/Chamber Uneven Temperature** | **PCB Failing Pattern** | | Chip Select Routing Defect | Horizontal | | Chip Clock/Address/Command Routing Defect | Vertical | | Hot Moisture Trap | Cluster | | Cooling Gradient | Edge at right hand side |   Common defects of each PCB board fail region. If it is related to moisture trap or cooling gradient, chamber temperature sensor data will be analyzed.    Simple illustration on temperature variation with time. Electrical current generates heat and the hot moisture can be trapped at certain corner. The temperature contrast increases with time. The embedded sensor inside the testing IC feedbacks the temperature after certain interval.  The test board report can also be used to forecast number of test board to test all the testing IC. The problematic board and false fails caused by machine defect can be forecasted.   |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | Time (Julian Week) | 01 | 02 | 03 | 04 | 05 | | Demand | 6000 | 2000 | 3000 | 5000 | 8000 |   Illustration of test chamber demand. The increment in fallout results in more oven usage. |
| **Requirements Overview:**  *Include what will be needed to carry out the project. You may describe any background knowledge that is needed or desired. You may also specify familiarity with specific programming language, tools or software platform that is needed or desired.*  *Python is used intensively in data extraction and implementation of the models and systems.*  ***Desired Outcome:***  *Be specific regarding the outcome of the project in terms of quantifiable and measurable deliverables unless it is very experimental project.*   1. Accuracy in predicting the chamber testing anomalies. 2. Accuracy in terms of true alarms generated by the system against the number of identified true cases. 3. Specificity and precision of the chamber test fail classification. 4. Accuracy in predicting test board failure. 5. Accuracy in finding chamber test that cause excessive die heating. (based on time series temperature sensor data) 6. Accuracy in predicting test board shortage based on IC testing demand (time series data)   ***Techniques under consideration:***  *You may describe certain techniques that will be needed or experimented with.*  Stacked integrated fuzzy neural network system. (Targeting on wafer and PCB board failing pattern)  PCA/LDA for dimensionality reduction as chamber testing result will be involved.  DTW (Targeting temperature sensor data and demand data which are time series.)  ***Project Risks:***  *You may also discuss some risks associated with the timely completion of the project.*  Data extraction requires additional time due to multiple testing results that creates a great number of features. |
| **Resource Requirements (please list Hardware, Software and any other resources)** |
| **Number of students required: (Please specify their tasks if possible)**  5 |
| **Methods and Standards:**  *Provide a brief overview of the approach to be taken, Verification & Validation methods, etc. This section should also state clearly the performance indicators to determine the success of the final system – for example, the system’s performance against human experts or industry standards, etc.*  In the industry, the chamber testing result is being analyzed by engineering team in order to refine the fabrication and assembly steps. It is a time-consuming project that takes a lot of engineering man-hours.  The chamber test result is also analyzed statistically in order to identify the out of control lots.  However, it is usual to have false alarm since the spatial region of the wafer is not being analyzed.  With the new system implemented, it will be helpful to automate recognition of the failing materials, equipment and tests that generate excessive current/heat. |

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| **Programme Name: IS/BA/SE** | **Project No:** | **Student Batch:** |
| **Accepted/Rejected/KIV:** | | |
| **Students Assigned:** | | |
| **Advisor Assigned:** | | |